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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,758	02/03/2004	Naoya Tsuchiya	11-220	8930

23400 7590 07/26/2005

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,758	TSUCHIYA ET AL.	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/3/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. An initiated copy of the information disclosure statement (IDS) submitted on 2/3/2004 is attached herewith.

Specification

3. The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. However, Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

Non-elected claims

4. The non-elected claims (claims 3-4) should be cancelled from the application when the elected claims (claims 1-2) are allowed or in response to this Office Action.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kasuya et al. (US 2001/0009389 A1).

Regarding claim 1, Kasuya et al. discloses an operational amplification circuit (Figs. 1-4) comprising a differential amplification circuit (50) and an outputting circuit (60), said differential amplification circuit including: a first input-stage transistor circuit (Tr54/Tr55) to which an input signal (-input) is inputted through an inverting input terminal; a second input-stage transistor circuit (Tr52/Tr53) to which an input signal (+input) is inputted through a non-inverting input terminal; third and fourth transistors (Tr58-Tr59) connected to said first and second input-stage transistor circuits, respectively, to constitute a current mirror circuit (see Fig. 4); a fifth transistor (Tr56) connected to a junction between said first input-stage transistor circuit and said third transistor; a sixth transistor (Tr57) connected to a junction between said second input-stage transistor circuit and said fourth transistor; and a current supply circuit (Tr50/Tr51) for supplying a current to said first and second input-stage transistor circuits and further for supplying a current to said fifth and sixth transistors, a current flowing in said sixth transistor being in proportion to the product of a current flowing in said fifth transistor, a ratio of current amplification factors of said third and four transistors and a ratio of current amplification factors of said fifth and sixth transistors, said outputting circuit (60) being made to output a low or high logical level on the basis of the relationship between said current to be supplied from said current supply circuit to said sixth transistor and said current flowing in said sixth transistor, said current supply circuit (Tr50/Tr51) being made such that, when the supply of said current to said first and second input-stage

transistor circuits comes to a stop, said current to be supplied to one of said fifth and sixth transistors increases while said current to be supplied to the other does not vary (see and compare the inventive Figures and the Figures above – they have the same structure or connection).

Regarding claim 2, Kasuya et al. discloses the current supply circuit is a multi-collector transistor including a first collector (Tr50/Tr51) connected to said first and second input-stage transistor circuits (Tr52-Tr55), a second collector connected to one of said fifth and sixth transistors (Tr56/Tr57) and a third collector connected to the other of said fifth and sixth transistors so that, when the supply of a current from said first collector comes to a stop, a portion of a current flowing in its emitter flows in said second collector (see and compare the inventive Figures and the Figures above).

Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see references cited on PTO-892 Form attached herewith).

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert (Bob) J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
July 20, 2005

PEGUY JEANPIERRE
PRIMARY EXAMINER